

Computer-Aided Interpretation of TFT Models

Xiang Cheng, Sungsik Lee, Guangyu Yao, and Arokia Nathan

The Hetero-Genesys Laboratory, Department of Engineering, University of Cambridge

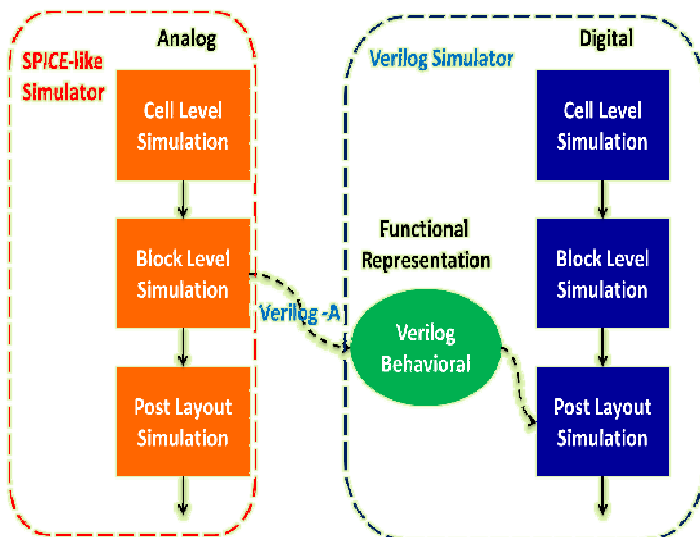
(E-mails: xc260@cam.ac.uk, an299@cam.ac.uk)

Introduction

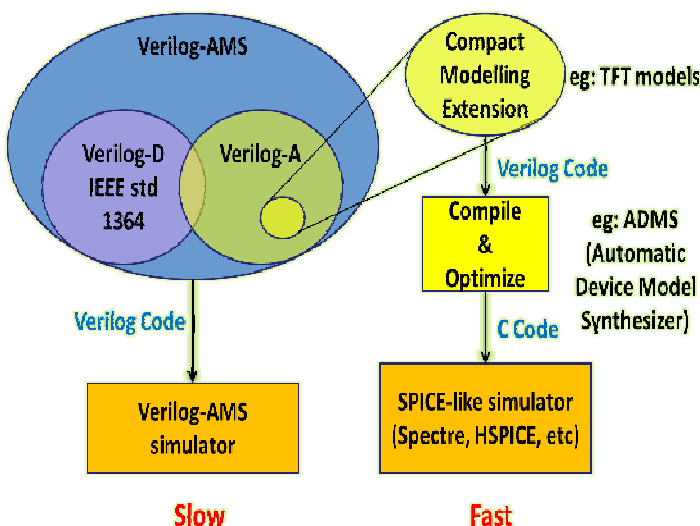
- SPICE and Verilog-AMS models compared in terms of their complexity and execution speed.
- Guideline in device modelling area while choosing the platform to implement their models.

Results and Discussions

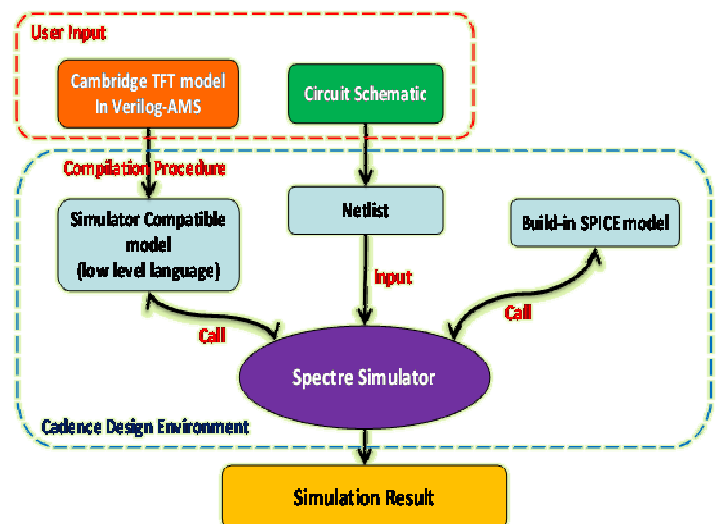
- Verilog-A behaviour model in early mixed signal simulation environment:



- Verilog-A(MS) extension for compact modelling with SPICE like simulator integration:



- Circuit design and simulation flow using Cambridge model in Cadence Design Environment:



- Comparison between different model languages:

Environments	SPICE	Verilog-AMS
Language	C/Fortran	Verilog
Language level	Low	High
Easy to use	No	Yes
Efficiency & Speed	High	Low
Complexity	High	Low
Simulator information	Simulation algorithm & limitations	None
Users	SPICE developers	End users

Conclusion

- Comparison the pros and cons of SPICE and Verilog-AMS in the aspect of device model development.
- Brief guideline in TFT modelling area to decide a modelling language proper to use.